IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application of	Atty. Docket: GB 020124
MARK J. CHILDS ET AL.	Group Art Unit: 2629
Serial No.: 10/523,379	Examiner: STUART S. MCCOMMAS
Filed: DECEMBER 14, 2005	CONF. NO.: 3728

TITLE: ELECTROLUMINESCENT DISPLAY DEVICE HAVING PIXELS WITH NMOS TRANSISTORS

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Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

APPEAL BRIEF

Sir:

Appellants herewith respectfully present its Brief on Appeal as follows:

REAL PARTY IN INTEREST

The real party in interest is Koninklijke Philips Electronics N.V., a corporation of The Netherlands having an office and a place of business at Groenewoudseweg 1, Eindhoven, Netherlands 5621 BA.

RELATED APPEALS AND INTERFERENCES

To the best of Appellants' knowledge and belief, there are no related appeals or interferences.

STATUS OF CLAIMS

Claims 1-16 are pending in this application. Claims 1-16 are rejected in the Final Office Action that issued July 11, 2008. This rejection was upheld, in an Advisory Action that mailed on September 29, 2008 in response to an Amendment After Final Action that was submitted on September 11, 2008. Claims 1-16 are the subject of this appeal.

STATUS OF AMENDMENTS

An Amendment After Final Action was submitted on September 11, 2008 in response to a Final Office Action mailed on July 11, 2008. The Amendment After Final Action did not include any amendments. In an Advisory Action mailed on September 29, 2008, it is indicated that the Request for Reconsideration, namely the Amendment After Final Action submitted on September 11, 2008, was considered but does not place the application in condition for allowance. This Appeal Brief is in response to the Final Office Action mailed on July 11, 2008, that finally rejected claims 1-16, which remain finally rejected in the Advisory Action mailed on September 29, 2008.

SUMMARY OF CLAIMED SUBJECT MATTER

The present invention, for example as claimed in claim 1, relates to an active matrix electroluminescent display device comprising an array of display pixels (e.g., see, present application, FIG. 3, 4 and accompanying description page 6, lines 24-26). Each pixel includes an electroluminescent display element (e.g., see, present application, display element 2, page 6, line 32 through page 7, line 1); an amorphous silicon or microcrystalline silicon first drive NMOS transistor connected between the anode of the display element and a power supply line (e.g., see, present application, drive transistor 22, page 6, line 30 through page 7, line 2); a storage capacitor between the anode of the display element and the gate of the first drive transistor (e.g., see, present application, storage capacitor 24, page 7, lines 3-4); and an amorphous silicon or microcrystalline silicon second drive NMOS transistor directly connected to the anode of the display element for supplying a holding voltage to the anode of the display element (e.g., see, present application, page 7, lines 13-16).

The present invention, for example as claimed in claim 9, relates to a method of driving the pixels of an active matrix electroluminescent display device comprising an array of display pixels (e.g., see, present application, FIG. 3, 4 and accompanying description page 6, lines 24-26) each having an electroluminescent display element (e.g., see, present application, display element 2, page 6, line 32 through page 7, line 1). The method includes holding the voltage across the display element by applying a holding voltage through a first amorphous silicon or microcrystalline silicon NMOS transistor directly connected to an anode of the electroluminescent display element (e.g., see, present application, drive transistor 22, page 6, line 30 through page 7, line 2), the holding voltage holding the source voltage of a second amorphous silicon or microcrystalline silicon NMOS transistor (e.g., see, present application, page 7, lines 13-16); while holding the voltage across the display element, storing a desired gate-source voltage on a storage capacitor connected between the gate and source of the second transistor, the gate-source voltage corresponding to a desired source-drain current for driving the display element (e.g., see, present application, storage capacitor

24, page 7, lines 3-4, 13-15, 23-29); removing the holding voltage from the display element (e.g., see, present application, page 7, lines 29-30); and driving the desired source-drain current through the electroluminescent display element (e.g., see, present application, page 7, lines 31-32, page 9, lines 3-4).

The present invention, for example as claimed in claim 14, relates to an active matrix electroluminescent display device comprising an array of display pixels (e.g., see, present application, FIG. 3, 4 and accompanying description page 6, lines 24-26). Each pixel includes an electroluminescent display element (e.g., see, present application, display element 2, page 6, line 32 through page 7, line 1); an amorphous silicon or microcrystalline silicon first drive NMOS transistor connected between the anode of the display element and a power supply line (e.g., see, present application, drive transistor 22, page 6, line 30 through page 7, line 2); a storage capacitor between the anode of the display element and the gate of the first drive transistor (e.g., see, present application, storage capacitor 24, page 7, lines 3-4); and an amorphous silicon or microcrystalline silicon second drive NMOS transistor directly connected to the anode of the display element

for supplying a holding voltage to the anode of the display element (e.g., see, present application, page 7, lines 13-16), wherein the gate of the first drive transistor is coupled to a data signal line through an address transistor (e.g., see, present application, page 7, lines 29-30), and wherein the first and second drive transistors comprise microcrystalline silicon TFTs comprising silicon crystallites of size 40 nm - 140 nm in an amorphous silicon matrix (e.g., see, present application, page 8, lines 25-28).

It should be explicitly noted that it is not the Appellants' intention that the currently claimed device and method be limited to operation within the illustrative device and method described above beyond what is required by the claim language. Further description of the illustrative device and method is provided above indicating portions of the claims which cover the illustrative device and method merely for compliance with requirements of this appeal without intending any further interpreted limitations be read into the claims as presented.

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Whether claims 1, 2, 5 and 15 of U.S. Patent Application Serial No. 10/523,379 are unpatentable under 35 U.S.C. §103(a) over U.S. Patent No. 6,734,636 to Sanford ("Sanford") in view of U.S. Patent Publication No. 2001/0002703 to Koyama ("Koyama '703").

Whether claims 3-7 of U.S. Patent Application Serial No. 10/523,379 are unpatentable under 35 U.S.C. §103(a) over Sanford in view of Koyama '703 in further view of U.S. Patent Publication No. 2001/0043168 to Koyama ("Koyama").

Whether claim 8 of U.S. Patent Application Serial No. 10/523,379 are unpatentable under 35 U.S.C. §103(a) over Sanford in view of Koyama '703 in further view of U.S. Patent Publication No. 2002/0105040 to Yamazaki ("Yamazaki").

Whether claims 9-13 and 16 of U.S. Patent Application Serial No. 10/523,379 are unpatentable under 35 U.S.C. §103(a) over Sanford in view of Koyama '703 in further view of U.S. Patent No. 6,809,706 to Shimoda ("Shimoda").

Whether claim 14 of U.S. Patent Application Serial No. 10/523,379 are unpatentable under 35 U.S.C. §103(a) over Sanford in view of Koyama '703 in further view of Yamazaki.

ARGUMENT

Claims 1, 2, 5 and 15 are said to be unpatentable over Sanford in view of Koyama '703.

Appellants respectfully request the Board to address the patentability of independent claim 1, and further claims 2, 5 and 15 as respectively depending from independent claim 1, based on the requirements of independent claim 1. This position is provided for the specific and stated purpose of simplifying the current issues on appeal. However, Appellants herein specifically reserve the right to argue and address the patentability of claims 2, 5 and 15 at a later date should the separately patentable subject matter of claims 2, 5 and 15 later become an issue. Accordingly, this limitation of the subject matter presented for appeal herein, specifically limited to discussions of the patentability of independent claim 1 is not intended as a waiver of Appellants' right to argue the patentability of the further claims and claim elements at that later time.

It is undisputed that "Sanford fails to disclose a transistor directly connected to the anode of the display element." (See, Final Office Action, page 3.) It must be pointed out that the claims do not merely recite "an amorphous silicon or microcrystalline silicon second drive NMOS transistor directly connected to the anode of the display element" as seems to be alleged by the Final Office Action. Claim 1 for example in pertinent part recites (emphasis added) "an amorphous silicon or microcrystalline silicon second drive NMOS transistor directly connected to the anode of the display element for supplying a holding voltage to the anode of the display element."

The Office Action states "that it was well known in the art to provide a transistor directly connected to the anode of the display element" and suggests that this is shown by Koyama '703. While the Applicants do not dispute that Koyama '703 shows a transistor 1409 connected directly to an anode of the display element 1405, it is strongly disputed that this is sufficient for rendering the claims as presented, as obvious over Sanford in view of Koyama '703. In fact, if Koyama '703 where utilized to modify Sanford as the Final Office Action stipulates is suggested, it is respectfully submitted

that this modification would render the circuit of Sanford inoperable. As taught in Sanford, it is the gate to source capacitance of Q302 (the second transistor in terms of the claim recitations) that is shown connected to the capacitor Cs310. Sanford teaches that it is this connection of Q302 to capacitor Cs310 (and not directly to the display element), which nulls out the gate to drain capacitance and thereby the voltage increase due to capacitive coupling from Q301 (see, FIG. 3 and the accompanying description contained in Col. 6, lines 50-59). If Q302 were connected directly to the anode of the display element as suggested in the Final Office Action, it is respectfully submitted that Q302 would not be enabled to null out the voltage increase from Q301 and accordingly, Q302 would not operate as it is intended by Sanford.

It is respectfully submitted that it is well settled that when a modification renders a device inoperative for its intended purpose, this modification is non-obvious. "If when combined, the references 'would produce a seemingly inoperative device,' then they teach away from their combination." (In re Sponnoble, 405 F.2d 578, 587, 160 USPQ 237, 244 (CCPA 1969). Further, there is no suggestion to modify a prior art reference where the modification

would render the device inoperable for its intended purpose. (In re Gordon, 733 F.2d 900 (Fed. Cir. 1984)). Since shifting the transistor Q302 to be directly coupled to the anode of the display element as suggested in the Final Office Action would render the transistor Q302 inoperative for counteracting the voltage increase from Q301, this suggestion is non-obvious and in fact it is well settled that this type of a modification, namely one that renders Q302 inoperative for its intended purpose, is taught away from by Sanford.

The Advisory Action maintains that "by directly connecting the additional transistor 1409 from Koyama to the anode of the EL element 1405 to supply any voltage including a holding voltage to the OLED precise gradation display can be achieved and picture quality can be improved." What is puzzling is that Koyama '703 does not disclose the transistor 1409 for improving picture quality to provide precise gradation display. Koyama '703 teaches the configuration of transistor 1409 to enable "two adjacent pixels [to] share one power source control line 1420." (See, "Koyama '703, paragraph [0170].) So now it appears that the Advisory Action is suggesting adding a second power line to the circuit of

Sanford. Yet in Sanford, there is only one power line as in Koyama '703. The benefit espoused by the Advisory Action is not recognized anywhere in any of the prior art and the configuration of multiple power lines is similarly not disclosed or even suggested.

Accordingly, the suggestion in the Final Office Action and Advisory Action that the combination of Sanford with Koyama '703 "would be obvious to one having ordinary skill in the art ... " is respectfully refuted. One may not utilize the teachings of the present application as a road map to selectively pick and choose amongst prior art references for the purposes of attempting to arrive at the presently disclosed invention. The Federal Circuit has identified three possible sources for motivation to combine references including the nature of the problem to be solved, the teachings of the prior art, and the knowledge of persons of ordinary skill in the art. (See, In re Rouffet, U. S. Court of Appeals Federal Circuit, U.S.P.Q. 2d, 1453, 1458.) There must be a specific principle that would motivate a skilled artisan, with no knowledge of the present invention, to add a further power supply line, when neither of Sanford with Koyama '703 disclose such a

circuit configuration. The use of hindsight in the combination of references is forbidden in comprising the case of obviousness. Lacking a motivation to combine references in the way suggested, a proper case of obviousness is not shown (see, In re Rouffet, 1458).

The Advisory Action states that Koyama '703 shows that the concept of directly connecting a transistor to the anode of Sanford is shown by Koyama '703. However, Koyama '703 nor Sanford show adding a second drive NMOS transistor directly connected to the anode of the display element for supplying a holding voltage to the anode of the display element as recited in claim 1.

Accordingly, it is respectfully submitted that the device of claim 1 is not anticipated or made obvious by the teachings of Sanford in view of Koyama '703. For example, Sanford in view of Koyama '703 does not disclose or suggest, a device that amongst other patentable elements, comprises (illustrative emphasis added) "an electroluminescent display element; an amorphous silicon or microcrystalline silicon first drive NMOS transistor connected between the anode of the display element and a power supply line; a storage capacitor between the anode of the display element and the gate of the first drive transistor; and an amorphous silicon or

microcrystalline silicon second drive NMOS transistor directly connected to the anode of the display element for supplying a holding voltage to the anode of the display element" as recited in claim 1. Koyama, Yamazaki and Shimoda are introduced for allegedly showing other elements of the claims and as such, do nothing to cure the deficiencies in Sanford in view of Koyama '703.

Based on the foregoing, the Appellants respectfully submit that independent claim 1 is patentable over Sanford in view of Koyama '703 and notice to this effect is earnestly solicited.

Claims 2, 5 and 15 respectively depend from claim 1 and accordingly are allowable for at least this reason as well as for the separately patentable elements contained in each of said claims. Accordingly, separate consideration of each of the dependent claims is respectfully requested.

Claims 3-7 are said to be unpatentable over Sanford in view of Koyama '703 in further view of Koyama.

Koyama is cited for allegedly showing elements of the dependent claims yet does not cure the deficiencies in each of

Sanford and Koyama '703. Claims 3-7 are allowable at least based on dependence from independent claim 1.

Claim 8 is said to be unpatentable over Sanford in view of Koyama '703 in further view of Yamazaki.

Yamazaki is cited for allegedly showing elements of the dependent claim yet does not cure the deficiencies in each of Sanford and Koyama '703. Claim 8 is allowable at least based on its dependence from independent claim 1.

Claims 9-13 and 16 are said to be unpatentable Sanford in view of Koyama '703 in further view of Shimoda.

Shimoda is cited for allegedly showing other element of the claims yet does not cure the deficiencies in each of Sanford in view of Koyama '703 as discussed above regarding claim 1. It is respectfully submitted that the method of claim 9 is not anticipated or made obvious by the teachings of Sanford in view of Koyama '703 in further view of Shimoda. For example, Sanford in view of Koyama '703 in further view of Shimoda does not disclose or

suggest, a method that amongst other patentable elements, comprises similar as recited with respect to claim 1, (illustrative emphasis added) "holding the voltage across the display element by applying a holding voltage through a first amorphous silicon or microcrystalline silicon NMOS transistor directly connected to an anode of the electroluminescent display element, the holding voltage holding the source voltage of a second amorphous silicon or microcrystalline silicon NMOS transistor; while holding the voltage across the display element, storing a desired gate-source voltage on a storage capacitor connected between the gate and source of the second transistor, the gate-source voltage corresponding to a desired source-drain current for driving the display element" as recited in claim 9.

Based on the foregoing, the Appellants respectfully submit that independent claim 9 is patentable over Sanford in view of Koyama '703 in further view of Shimoda and notice to this effect is earnestly solicited.

Claims 10-13 and 16 are allowable at least based on dependence from independent claim 9.

Claim 14 is said to be unpatentable over Sanford in view of Koyama '703 in further view of Yamazaki.

Yamazaki is cited for allegedly showing other elements of the claim yet does not cure the deficiencies in each of Sanford and Koyama '703 as discussed above regarding claim 1. It is respectfully submitted that the device of claim 14 is not anticipated or made obvious by the teachings of Sanford in view of Koyama '703. For example, Sanford in view of Koyama '703 does not disclose or suggest, a device that amongst other patentable elements, similar as the device in claim 1, comprises (illustrative emphasis added) "an electroluminescent display element; an amorphous silicon or microcrystalline silicon first drive NMOS transistor connected between the anode of the display element and a power supply line; a storage capacitor between the anode of the display element and the gate of the first drive transistor; and an amorphous silicon or microcrystalline silicon second drive NMOS transistor directly connected to the anode of the display element for supplying a holding voltage to the anode of the display element" as recited in claim 14.

Based on the foregoing, the Appellants respectfully submit that independent claim 14 is patentable over Sanford in view of Koyama '703 in further view of Shimoda in further view of Yamazaki and notice to this effect is earnestly solicited.

In addition, Appellants deny any statement, position or averment of the Examiner that is not specifically addressed by the foregoing argument and response. Any rejections and/or points of argument not addressed would appear to be moot in view of the presented remarks. However, the Appellants reserve the right to submit further arguments in support of the above stated position, should that become necessary. No arguments are waived and none of the Examiner's statements are conceded.

CONCLUSION

Claims 1-16 are allowable over Sanford alone and in view of any of Koyama in view of Koyama 703 alone and in view of any combination of Koyama, Yamazaki and Shimoda.

Thus the Examiner's rejection of claims 1-16 should be reversed.

Respectfully submitted,

By _____
Gregory L. Thorne, Reg. 39,398
Attorney for Appellants
December 10, 2008

THORNE & HALAJIAN, LLP
Applied Technology Center
111 West Main Street
Bay Shore, NY 11706
Tel: (631) 665-5139
Fax: (631) 665-5101

APPENDIX A

CLAIMS ON APPEAL

1. (Previously presented) An active matrix electroluminescent display device comprising an array of display pixels, each pixel comprising:

an electroluminescent display element;

an amorphous silicon or microcrystalline silicon first drive NMOS transistor connected between the anode of the display element and a power supply line;

a storage capacitor between the anode of the display element and the gate of the first drive transistor; and

an amorphous silicon or microcrystalline silicon second drive NMOS transistor directly connected to the anode of the display element for supplying a holding voltage to the anode of the display element.

2. (Previously presented) A device as claimed in claim 1, wherein the second drive transistor is connected between the power supply line and the anode of the display element.

3. (Previously presented) A device as claimed in claim 1, wherein the second drive transistor is connected between a second power supply line and the anode of the display element.

4. (Previously presented) A device as claimed in claim 3, wherein the second power supply line is shared between pixels in a row of the array.

5. (Previously presented) A device as claimed in any one of claims 1 to 4, wherein the gate of the first drive transistor is coupled to a data signal line through an address transistor.

6. (Previously presented) A device as claimed in claim 1, wherein the gate of the first drive transistor is coupled to a data signal line through an address transistor, and wherein the data signal line comprises a column conductor shared between pixels in a column of the array.

7. (Previously presented) A device as claimed in claim 6, wherein the gate of the address transistor is coupled to a row conductor shared between pixels in a row of the array.

8. (Previously presented) A device as claimed in claim 1, wherein the first and second drive transistors comprise microcrystalline silicon TFTs comprising silicon crystallites of size 40 nm - 140 nm in an amorphous silicon matrix.

9. (Previously presented) A method of driving the pixels of an active matrix electroluminescent display device comprising an array of display pixels each having an electroluminescent display element, the method comprising:

holding the voltage across the display element by applying a holding voltage through a first amorphous silicon or microcrystalline silicon NMOS transistor directly connected to an anode of the electroluminescent display element, the holding voltage holding the source voltage of a second amorphous silicon or microcrystalline silicon NMOS transistor;

while holding the voltage across the display element, storing a desired gate-source voltage on a storage capacitor connected between the gate and source of the second transistor, the gate-source voltage corresponding to a desired source-drain current for driving the display element;

removing the holding voltage from the display element; and

driving the desired source-drain current through the electroluminescent display element.

10. (Previously presented) A method as claimed in claim 9, wherein the desired source-drain current is driven through the second transistor by applying a first power supply voltage to the second transistor.

11. (Previously presented) A method as claimed in claim 10, wherein the first power supply voltage is not applied to the second transistor while the voltage across the display element is held.

12. (Previously presented) A method as claimed in claim 11, wherein the first power supply voltage and the holding voltage are provided by a shared power supply line.

13. (Previously presented) A method as claimed in any one of claims 9 to 12, wherein storing a desired gate-source voltage on a storage capacitor comprises coupling data from a data signal line to the storage capacitor through an address transistor.

14. (Previously presented) An active matrix electroluminescent display device comprising an array of display pixels, each pixel comprising:

an electroluminescent display element;

an amorphous silicon or microcrystalline silicon first drive NMOS transistor connected between the anode of the display element and a power supply line;

a storage capacitor between the anode of the display element and the gate of the first drive transistor; and

an amorphous silicon or microcrystalline silicon second drive NMOS transistor directly connected to the anode of the display

element for supplying a holding voltage to the anode of the display element, wherein the gate of the first drive transistor is coupled to a data signal line through an address transistor, and wherein the first and second drive transistors comprise microcrystalline silicon TFTs comprising silicon crystallites of size 40 nm - 140 nm in an amorphous silicon matrix.

15. (Previously presented) A device as claimed in claim 1, wherein a cathode of the electroluminescent display element is directly connected to ground.

16. (Previously presented) A method as claimed in claim 9, wherein a cathode of the electroluminescent display element is directly connected to ground.

APPENDIX B

Evidence on Appeal

None

APPENDIX C

Related Proceedings of Appeal

None